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Method of performing Design FMEA on electronic circuit diagrams

Keywords

electronic circuit analysis, failure mode, TTAA

Abstract

Existing method of performing FMEA for electronic diagrams is time consuming task. For complex systems analysis of every single component failure mode and its effect deeply involves design team and blocks resources availability for long time. Method presented in this paper allows effective analysis of design failure modes using FMEA approach carrying so called Time to Acceptable Analysis (TTAA) constraint.

1. Introduction

Performing Failure Mode and Effect Analysis of the Design (DFMEA) in adequate product development time, is desired and becomes required task of every electronic products design process. Output from analysis shall provide the list of risk mitigation procedures (Recommended Actions) with their appropriate description. Current approach is based on part by part analysis, which has one major disadvantage – is very time and resources consuming. And Time to Acceptable Analysis (TTAA) measure, which corresponds to the period of time from the beginning of analysis to the satisfactory report is very long [1]. Approach described in this paper is useful especially for analysis designs with large number of components/elements. More than 200 of components/elements seems to be reasonable of performing such kind of analysis where TTAA is important. We can't avoid simplifications even in low components number circuits with Large Scale Integreation (LSI) components on the board. Integrated circuits manufacturers usually provides block diagram of internal IC structure instead of complete schematic, that keeps the structure know-how on manufacturer side. The only available data for designer are the electrical parameters of inputs and outputs and their functionality depending on the components type.

2. Requirements to design documentation

In order to make design documentation more transparent - especially in regards to complex electronic circuits - one of the good practice is to divide the circuit diagram into functional blocks, with component groups limited to those which allows to perform particular function.

As shown in *Figure 1* circuit components are grouped into functional blocks and are connected with others functional blocks logically. Usually in electrical diagrams lines represents electrical connection formed in reality by PCB copper path or wire. Jumpers or connectors should be represented as a separate parts. Such approach can be depicted even simpler using functional blocks and their interconnections or interfaces as it is described in chapter 3. It can be easily implemented at the beginning of circuit design process, which starts usually from system architecture definition. All electrical signals exchanged between functional blocks shall have unique name in order to ease the identification during analysis.

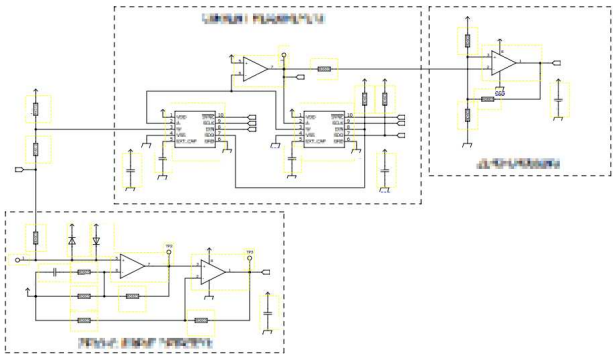

Figure 1. Circuit diagram partitioning example

3. Creating input to analysis

In order to make analysis efficient, some preparation is required in advance. Prerequisites are:

1. *Operating temperature*
   Most electronic devices are sensitive to temperature changes, which influences their parameters. Temperature range to which analyzed design is exposed, must be clearly defined

2. *Electromagnetic field exposition*
   Some of electronic devices are sensitive to external electromagnetic fields. Having information about possible exposure can be essential during analysis execution.

3. *Vibrations*
   In case of vibrations some components can lost their connections to PCB or leads. The most susceptible to such kind of failure modes are components with high inertia, due to their size and weight like electrolytic capacitors, transformers. Also direction of stress (vibration axis vs component axis) shall be taken into consideration, in regards to the failure mode probability of occurrence.

Besides mentioned points, some effort is required in regards to signals interfacing blocks. All requirements allocated to the signals should be listed, and the requirements depends on the signal type and it's properties. *Table 1* shows exemplary set of information describing particular signals.

In addition to the table recommended practice is to prepare overview of design structure using functional blocks and their interfaces as listed in *Table 1*. As an example *Figure 2* shows such kind of design structure with blocks. Additional colors assigned to blocks shows their affiliation with any of general functionality (e.g. measurement stage or Power Supply stage).

Table 1. Signal description table

Signal name	Type	Low value	Nominal value	Max value
V_{OUT_CAP}	Voltage	120V	140V	160V
V_{CTRL}	PWM	4.5V/20%	5V/60%	5.5V/95%
V_{OUT_CAP}	Pulsation can't exceed 0,1V p-p			
V_{CTRL}	Rise/fall time >10us			

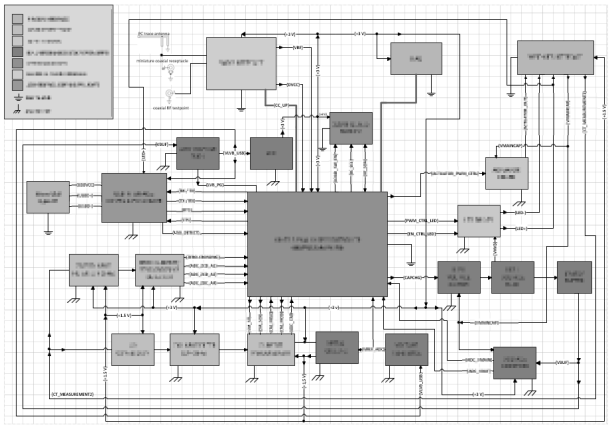

Figure 2. Circuit partitioning functional block diagram

4. Performing the analysis

After collecting of all necessary documents and performing required steps, to start the analysis recommendation from [2] should be fulfilled. Design team, service, system representative should attend in order to ensure high quality and efficiency of the analysis. As an example, structure shown in *Figure 3*. is used as an object for analysis.

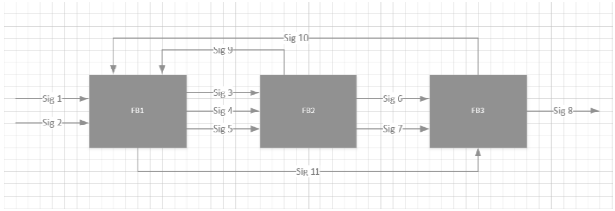

Figure 3. Example blocks connection logic

During the analysis one general assumption is followed: inputs of every functional block is within its limits and doesn't introduce any unpredictable values. Worst case scenarios or failure modes should be assigned to the functional blocks output signals, and their propagation should be analyzed in order to get right logical End Effect. The only exceptions are external signals connected to particular blocks. This should be treated as an integral part of functional block with possible failure modes. For example let's analyze FB1. Starting analysis from 1st output signal "Sig 3" all failure modes connected to this signal shall be considered. Example failure modes for voltage driven output are:
- Lack of Sig 3
- Too low rise time at startup
- Overshoots at startup
- Signal level changes out of limit
- To high signal level.

Part / Module	Function	Potential Failure Modes	Potential Effect(s) of Failure	S E V	Potential Cause(s) / Mechanism(s)	O C C	Current Design Control Prevention	Current Design Control Detection	D E T	Risk (Sev*Occ)	R P N	Recommended Action(s)
										0	0	
										0	0	
										0	0	
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Figure 4. Design FMEA template

Every failure mode shall then be analyzed with top-down approach, looking for causes resulting in failure mode occurrence. In addition bottom up analysis shall be performed in order to find the worst case of End Effect. In this example Sig 3 disturbances caused by internal failure of FB1 will influence FB2, and indirectly itself due to presence of Sig 9. Sig 9 failure can propagate via Sig 11 to FB3 or via incorrectly driven FB2 causing finally incorrect value of Sig 8 which in this case is an output of the circuit. During the analysis of FB1 structure independently of its function, besides engineers experience it is good to have failure modes fraction of electronic devices used in FB1. These information are accessible either from standards [3] or from databases collecting this type of information [4]. Exemplary use of FMEA template is shown on *Figure 4.*

Following the rules described below we have:
Part/Module**:** *FB1*
Function**:** e.g.: *Provide Sig 3 within the desired value* (here should be listed all the necessary signal parameters)
Potential Failure Modes**:** List the failure modes the signal/block can be affected with – see examples bellow
Potential Causes/Mechanism: The list of component/subcircuit failure modes or variances which can influence the output property or function described in the *Function* row. The list of causes can be as long as required, until all list of identified suspicious points will be exhausted.

Potential causes can be taken from e.g. FMD2013 [4] providing failure modes of electronic components and their fraction of the failure rate. As an example diode failure modes taken from FMD2013 database are shown in *Table 1.*
In order to determine influence of the element to the output, one shall consider its failure modes and their occurrence likelihood as well as significance of their influence to the output. Based on the analysis results, corresponding prevention/detection recommendation can be addressed to the design team and considered for further design evaluation.

Table 1. FMD-2013 Zener Diode Failure modes list with Alpha friction from FMECA

#	Failure Mode	
	Description	**Alpha**
1	Induced Failure	0.5820
2	Electrical Overstress	0.1190
3	Opened	0.0900
4	Shorted	0.0750
5	Drift	0.0450
6	Seal Failure	0.0450
7	Voids	0.0450

5. Conclusions

All considerations presented in the paper shall be executed in the right point of time allowing design team to introduce changes/recommendations before type tests/product validation. Design team shall be experienced due to the need of parts screening. And part screening requires deep understanding of circuit operation principles being analyzed, as well as technical limitations related to assembly process. Prior to analysis start, it is vital to verify company service database for any available data concerning failure modes and claims submitted either internally or externally related to similar application.

References

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